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Dynamic Characteristics of Mho Distance Relays

DYNAMIC CHARACTERISTICS OF MHO DISTANCE RELAYS

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ABSTRACT

This paper describes the dynamic characteristic of phase mho relays which use the faulted phase voltage as the polarizing quantity, and which have "memory action" in the polarizing circuit. The dynamic characteristic begins as a large circle whose diameter is determined by the equivalent source impedance behind the relay, and then shrinks to the steady-state mho circle as the memory action decays. This provides much more fault resistance capability for close-in faults than is indicated by the steady-state characteristic.

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INTRODUCTION

For many years phase mho distance relays, of both electromechanical and static design, have used memory action to produce a short duration output for zero voltage faults at the relay location. The polarizing circuit contains a tuned circuit and, in effect, "remembers" the prefault voltage long enough for the relay to make a decision as to whether the fault is in front of, or behind, the relay. Usually the relay output lasts for only a few cycles and then the relay resets, since it is impossible for it to produce a steady state tripping output if the polarizing voltage is zero.

The above explanation of memory action is usually associated with zero voltage, or bolted, faults. However, in many cases fault impedance exists due to the presence of an arc, and the voltage is not zero. The memory action actually produces a dynamic characteristic that has a much greater capability to handle high-resistance close-in faults than is indicated by the steady-state characteristic. The purpose of this paper is to describe this dynamic characteristic.

It should be emphasized that this is not a new development, but is a description of a feature that is present in any mho relay which uses the faulted phase voltage as the polarizing voltage and which also uses memory action in the polarizing circuit. (1)

THEORY OF OPERATION

Relay Circuitry

This analysis refers to one relay unit of a three-phase mho distance relay, for example the AB phase pair unit. Phase distance relays normally use line-to-line voltage, V_{AB}, and "delta currents," $I_A - I_B$, so that the reach is the same in positive sequence ohms for phase-to-phase or three-phase faults.

This analysis is based on a static mho distance relay, such as the SLY51B (used in static terminals), which uses a phase angle comparator to make a distance measurement. The measuring unit for the AB phase pair is shown schematically in Fig. 1. The current input, $I_A - I_B$, is passed through a replica impedance, Z_R, which determines the reach and the maximum reach angle of the mho measurement. The voltage input, V_{AB}, is used both as the restraint portion of the operating signal and as the polarizing signal.

In the polarizing circuit, the memory circuit is a band-pass filter tuned to the system frequency. If the input signal to the filter is suddenly short-circuited, as would happen for a nearby bolted fault, the memory circuit will continue to oscillate for several cycles at system frequency. If the fault is nearby and contains fault resistance, the voltage V_{AB} will be reduced and phase-shifted to a position in phase with the fault current, and the phase shift of the memory circuit output will be delayed for several cycles.

For the standby condition with no load or fault current flowing, the operating signal, V_{OP}, is 180° out of phase with the polarizing voltage, and for this condition there is no input to the coincidence timer. If a phase-to-phase AB fault with no fault resistance occurs within the reach of the relay, and if the angle of Z_R is equal to the line angle, $(I_A - I_B)Z_R$ will be greater than V_{AB}, V_{OP} will be in phase with V_{POL}, and the input to the coincidence timer will be a chain of coincidence blocks that are almost one-half cycle long, with very narrow gaps between the blocks (see Fig. 2). This will produce a trip output.

If fault resistance is present, V_{OP} will not be in phase with V_{POL}, and operation of the relay will occur when the coincidence timer input blocks are greater than 90°. Fig. 3 illustrates by means of an JR-IX diagram the way in which a phase angle measurement produces a steady-state mho characteristic. Regardless of the angle between V_{AB} and I (or I_R), the 90° relationship between V_{OP} and V_{AB} required for operation causes the resulting characteristic to be a circle. Output occurs when the angle θ is equal to or less than 90°, or when the tip of the V_{AB} phasor falls within the circle. Dividing the voltages by I produces a mho circle on an R-X diagram, and operation occurs when Z_F falls within the circle.

Dynamic Characteristic

The dynamic characteristic of the mho relay with memory action is the result of the delay (in the memory circuit) of the phase shift of the polarizing voltage from the prefault to the fault condition.

To illustrate the dynamic characteristic, consider the simple radial feed system of Fig. 4, where impedances are given in secondary ohms. The source impedance is 6 ohms at 85° and the line impedance from relay location to fault location is 2 ohms at 85°. The fault resistance is assumed to have a value of 5 ohms, which is much larger than typical arc resistance values. This large value of fault resistance is used only to illustrate the size of the dynamic characteristic.

For the prefault condition the voltages at the source (V_S), at the relay (V_R), and at the point on the line where the fault occurs (V_X) are all in phase and equal to the source voltage as shown in Fig. 4. When the fault occurs, the voltage at the relay location shifts lagging by 33°, and the voltage across the fault resistance is in phase with the fault current and lagging by 54°, as shown at the bottom of Fig. 4.

Fig. 5 is a phasor diagram with source voltage, V_S, as the reference. Note that the voltage drop in the source impedance leads the source voltage by 31° and that the voltage drop from the relay to the fault, which is the same as V_{AB} at the relay, lags the source voltage by 33°.

When the phasor diagram of Fig. 5 is plotted on an IR-IX diagram it appears as shown on Fig. 6, with all the phasors rotated clockwise by 36°. V_{AB} at the source is the initial polarizing voltage, and V_{AB} at the relay terminals is the restraint portion of the V_{OP} signal, and therefore immediately after the fault occurs these two voltages are different as shown in Fig. 6. The angle θ is measured between V_{OP} and V_{AB} at the source and this produces an initial dynamic characteristic as shown in Fig. 6. The angle of Z_R was chosen to be the same as the source impedance angle, and the magnitude of Z_R was chosen to produce a circle which passes through the tip of the $V_{AB} = IZ_F$ phasor. This construction

illustrates the point that the diameter of the initial dynamic characteristic circle is equal to Z_S (source impedance) plus Z_R (relay reach). It also illustrates the point that the dynamic characteristic has a much greater reach along the R-axis than does the steady-state characteristic.

It might appear at first glance that this characteristic is no longer directional because it includes a large area below the R-axis. This is not true, because the construction of Fig. 6 is only valid for current flow through the source impedance behind the relay and passing through the relay location in the tripping direction. The area below the axis would permit tripping on a dynamic basis for capacitive faults in front of the relay (if series capacitors are used) but it does not mean that the relay would operate for faults behind the relay.

The dynamic characteristic as shown in Fig. 6 is the characteristic that exists immediately after the inception of the fault. Following fault inception, the characteristic begins to "shrink" towards the steady-state characteristic as shown in Fig. 7. The particular characteristic which determines the actual reach along the R-axis depends on the operating time of the relay. As far as the polarizing voltage itself is concerned, the time for V_{AB} to shift from the prefault to the fault position is determined by the memory circuit time constant and the magnitude of the fault voltage present during the fault at the input to the memory circuit. In general, this time constant is designed to be long enough to provide a trip output for "practical" faults in the first quadrant, i.e. faults with arc-drop.

Arc-Drop Considerations

A practical fault between phases A and B will have a non-linear fault resistance established by the fault arc. Since the arc voltage if relatively constant for all values of fault current, being typically 4 to 5% of V_{AB}, the fault resistance is inversely proportional to the fault current. However, the fault current is inversely proportional to the line and source impedance between the fault location and the infinite bus behind the relay. The net result is that fault resistance due to arc drop increases as the source impedance and relay dynamic characteristic diameter increases, and conversely the fault resistance decreases as the source impedance and relay dynamic characteristic diameter decrease.

This relationship is illustrated in Fig. 8 and Fig. 9. Figure 8 shows the practical fault impedance that will occur for a phase-to-phase fault at location R. (IZ_{1S} + IZ_F) is equal to the prefault voltage and IR_F is equal to 5% of the prefault voltage. Therefore R_F is equal to approximately 5% of (Z_{1S} + Z_F) Fig. 9 shows the same fault condition but with a smaller source impedance and therefore a smaller RF for a fault at the same fault location. It is interesting to note that in both of these conditions, even with an 85° reach angle on the steady state characteristic, the fault impedance is well within the dynamic characteristic, and that the dynamic characteristic automatically increases in size as the fault resistance increases.

Because the arc-drop voltage is essentially constant, infeed from the opposite terminal that is in-phase with the local fault current does not change the effective fault resistance seen by the local relay. Therefore Figures 8 and 9 apply to both double-end feed or single-end feed conditions provided that the two source impedances are in-phase.

Effects of Load Flow

For most applications, on lines that are part of a strong system, there will be no significant effect on the dynamic characteristic due to load flow. The key factor is the difference in angle between the pre-fault voltage at the relay location and the voltage at the equivalent source which is driving the fault current.

A system condition which could have a significant effect on the dynamic characteristic is shown in Fig. 10, where several transmission lines in series connect a generating station (A) at the left with a load center (B) at the right. Z_D is the positive sequence impedance between A and Bus 1, Z_E is the positive sequence impedance between Bus 1 and Bus 2, etc. R_1, R_2, and R_3, etc. are relay locations. The angular relationship of each bus voltage with respect to source A is shown below each bus location. F_1, F_2, F_3, etc. are fault locations in front of each relay location. For simplicity, it is assumed that the relay replica impedance angle is the same as the impedance angle of the various line sections, and that this angle is 85°.

To explain the effect of load angle on the dynamic characteristic, consider first the relay at location R_1. The source of fault current flow at R_1 for a fault at F1 is the voltage at A, but the prefault voltage at R_1 lags that voltage by 5°. In the previous description of the dynamic characteristic, for the no-load condition, the prefault voltage was the same as the source voltage, and the dynamic characteristic was much larger than the steady-state because the prefault voltage angle was leading with respect to the fault voltage. In the case of the R_1 relay of Fig. 10, the initial polarizing voltage lags the source voltage by 5°, and this will cause a slight reduction in the first quadrant reach along the R-axis.

Fig. 11 illustrates the effect of the load angle on the dynamic characteristic. The source impedance plus the relay reach form a "constant chord" for both characteristics. If the angle subtended by the no load characteristic is 90°, the angle subtended on the load characteristic is 90° + δ where δ is the angle that the prefault voltage at R_1 lags the voltage at the source A. The same effect applies at the other relay locations. For example, for the relay at R3 the subtended angle is 90° + 25° or 115°. This characteristic is illustrated in Fig. 12.

For a condition such as this the dynamic characteristic can be shifted to the right by introducing a fixed leading phase shift in the polarizing voltage, provided that the load flow is always in the same direction. Of course, this also shifts the steady-state characteristic toward the R-axis, or to a lower maximum reach angle.

For relay locations, such as R_4, R_5, and R_6, where the direction of load current flow is opposite to the direction of fault current flow, the shift of the dynamic characteristic because of load flow angle is in the opposite direction, or such that it takes in more area in the first quadrant.

A more direct method of evaluating relay performance is shown in the next series of figures. Since the item of chief concern is the ability to detect a fault with fault resistance and located just in front of the relay, these figures show the voltage phasors for V_{OP} and the initial polarizing voltage for faults at F1, F2 and F3. In each case it is assumed that I lags the left source voltage by 85°, so that IZ in the relay is in phase with the source voltage at the left.

In Fig. 13a, for the R_1 relay and F1 fault, the arc voltage is small compared to IZ, and V_{OP} leads IZ by 2°. V_{POL} lags the source voltage by 5°, so the angle between V_{OP} and V_{POL} is 7°, a very favorable angle for high-speed operation.

Fig. 13b shows the phasors for the R_2 relay and F2 fault. For this case, the arc voltage is a larger percentage of the IZ signal, and V_{OP} leads IZ by 5°. V_{POL} lags IZ by 15° resulting in a total angular separation of 20° between V_{OP} and V_{POL}.

Fig. 13c shows the phasors for the R_3 relay and F3 fault. The arc voltage is a still larger percentage of IZ and shows a phase shift in the clockwise or lagging direction due to the infeed to the fault from the right hand source. The total angle between V_{OP} and V_{POL} is 38°. While this is still well under 90° it is a less favorable condition than that for R_2 and F2, and, as stated earlier, could be improved by introducing a fixed leading phase shift of the polarizing voltage, provided the load flow direction is always the same.

Fig. 13d shows the input signals for the R_6 relay and F6 fault, which is the condition where load flow direction and fault current flow are opposite. Here V_{POL} leads IZ (and the right hand source voltage) by 20° but is only 15° away from V_{OP} because V_{POL} and V_{OP} are both shifted in the same direction from IZ. This is a favorable condition.

Figs. 13a, 13b, and 13c illustrate another important point. As the fault location moves towards the right-hand bus, the arc voltage shifts in the lagging direction because the amount of current fed in from the right increases. The V_{ARC} phasor shown in Fig. 13c for example, is the minus V portion of IZ — V. The steady-state polarizing voltage is 180° from the V_{ARC} shown, and is therefore more than 90° from V_{OP}, which means that the relay with 85° maximum reach angle will not operate steady-state for this fault. This is illustrated in Fig. 14. In this case the dynamic characteristic is relied upon to produce an output.

Performance on Reverse Direction Faults

Since the dynamic characteristic is generally larger than the steady-state characteristic, it is important to consider the performance of a mho relay with memory action when reverse direction external faults occur.

(1) Radial Case

Consider first the simple radial case as shown in Fig. 15, with a reverse direction fault just beyond the relay location. If the impedance angle of the source plus line impedance is 85°, the fault current lags the source voltage by 85°, and the arc drop (voltage at the relay location) lags the source voltage by 85° also. The current through the relay is 180° from the arc drop, and IZ_R (assuming an 85° transactor angle) is 180° from the source voltage. VOP differs from IZ_R by the arc drop voltage.

As shown in the phasor diagram of Fig. 15, the angle between V_{OP} and the initial polarizing voltage is approximately 165°. As the memory action decays, the polarizing voltage shifts lagging to the steady-state (V_{ARC}) position, giving a final steady-state angle that is smaller but that is still greater than 90°. Therefore the relay has less tendency to operate under the dynamic (initial)

condition than it does steady-state, and it does not operate under either dynamic or steady-state conditions.

(2) Load Flow in Tripping Direction

Fig. 16 shows the effect of load flow in the tripping direction, using the same system conditions as in Fig. 10. Consider the R1 relay and the F4 fault location since this gives the greatest angular difference between the voltage driving the fault current and the prefault, or initial, polarizing voltage. In this case the relay current is driven by a voltage that lags the initial polarizing voltage. As a result, both the dynamic and steady-state angles between V_{OP} and V_{POL} are considerably more than 90°, and therefore the relay does not operate.

(3) Load Flow in Non-Tripping Direction

Fig. 17 shows the effect of load flow in the non-tripping direction. Consider the R4 relay and the F5 fault location, again in the system of Fig. 10. The driving voltage for the fault current now leads the initial polarizing voltage, and IZ_R is shifted leading by approximately 60° compared to its position in Fig. 16. The dynamic angle is much greater than 90°, a good non-tripping condition, but the steady-state angle is slightly less than 90° and could produce a trip output if the arc voltage is above the sensitivity level of the polarizing circuit.

While this steady-state condition has the possibility of producing a false trip on a delayed basis, after the memory action has decayed, these points should be kept in mind:

(a) This is a "special case" requiring a wide angular separation between the two sources, and a relay location near a strong source at the receiving end of the system.
(b) The separation angle is just slightly less than 90°, and therefore the relay operation may be slow enough for the fault to be cleared before it trips.
(c) If the load flow is always in this direction, the polarizing voltage could be shifted more leading (or the IZ voltage more lagging) to prevent operation.

The important point is that this is a steady-state problem, and that the same dynamic characteristic which provides a greater tendency to trip, compared to steady-state, on internal faults, also provides a greater tendency not to trip on reverse direction faults.

Performance of Zone 1 Relay for Line-End Fault

A further consideration in the application of Zone 1 distance relays is the security against over-reaching on faults just beyond the remote end of the line.

(1) No Load Flow

Fig. 18 illustrates a simple case with no load flow. The angle between the initial polarizing voltage and the operate voltage (dynamic angle) is less than the angle between the final polarizing voltage and the operate signal (steady-state angle). However, both angles are significantly larger than the 90° or less required for operation, and this provides ample security.

(2) Load Flow in Non-Tripping Direction

Fig. 19 illustrates the separation angles obtained for the relay at R6 for a fault at F4 with load flow

in the non-tripping direction. Again the dynamic angle is less than the steady-state angle and there is significant safety margin above the 90° angle required for operation.

(3) Load Flow in Tripping Direction

Fig. 20 illustrates the separation angle obtained for relay R3 for a fault at F5, with load flow in the tripping direction. Load flow in this direction reduces both the dynamic and steady-state angles compared to the no-load case. The dynamic angle is larger than the steady-state angle, and both are greater than 90°, preventing mis-operation. It should be noted, however, that if a leading phase shift were to be used in the polarizing circuit of R3 to improve performance for close-in faults, it would decrease the separation angle for remote bus faults, with increasing risk of overreaching.

To summarize, then, in the first two cases above there is adequate security against overreaching under both dynamic and steady-state conditions. In the third case, where separation angles are closer to 90°, the dynamic characteristic provides more security against overreaching than does the steady-state characteristic.

Other Polarizing Methods

It is possible to use the "healthy-phase" voltage as the polarizing voltage, either alone or as a supplement to the faulted phase voltage, and by this means obtain a steady-state output for zero-voltage phase-to-phase faults. The latest designs of GE phase mho relays use a combination of faulted phase and unfaulted phase voltage, and the design of these relays will be described in a subsequent paper. With this polarizing method, the dynamic characteristic is still relied upon to produce an output for three-phase faults.

CONCLUSIONS

The use of a memory circuit in mho distance relays gives those relays a dynamic characteristic with much greater reach along the R-axis than the steady-state reach. The diameter of the initial dynamic characteristic is equal to the sum of the source impedance and the relay reach. The diameter automatically increases in size as arc resistance increases. The dynamic characteristic "shrinks" to the steady-state characteristic at a rate determined by the time constant of the memory circuit. The dynamic characteristic permits tripping on a transient basis for some marginal conditions that would not provide a steady-state trip output. The dynamic characteristic does not increase the risk of tripping incorrectly for reverse direction faults, nor the risk of overreaching for forward direction faults.

REFERENCES

1. L. M. Wedepohl, "Polarized Mho Distance Relay." Proceedings of IEE, Volume 112, No. 3, March 1965.

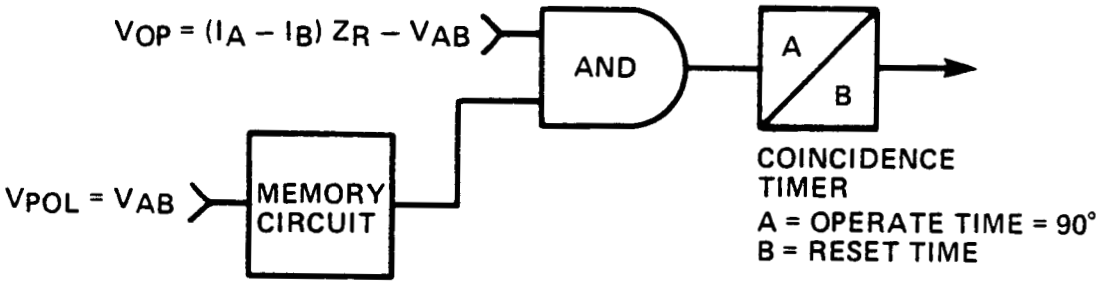


Fig. 1 Phase Angle Comparator Mho Distance Relay for the AB Phase Pair

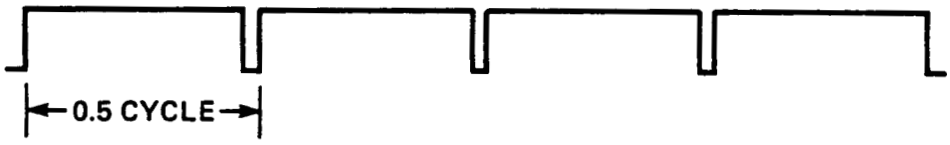


Fig. 2 Chain of Coincidence Blocks for Internal Fault with No Fault Resistance

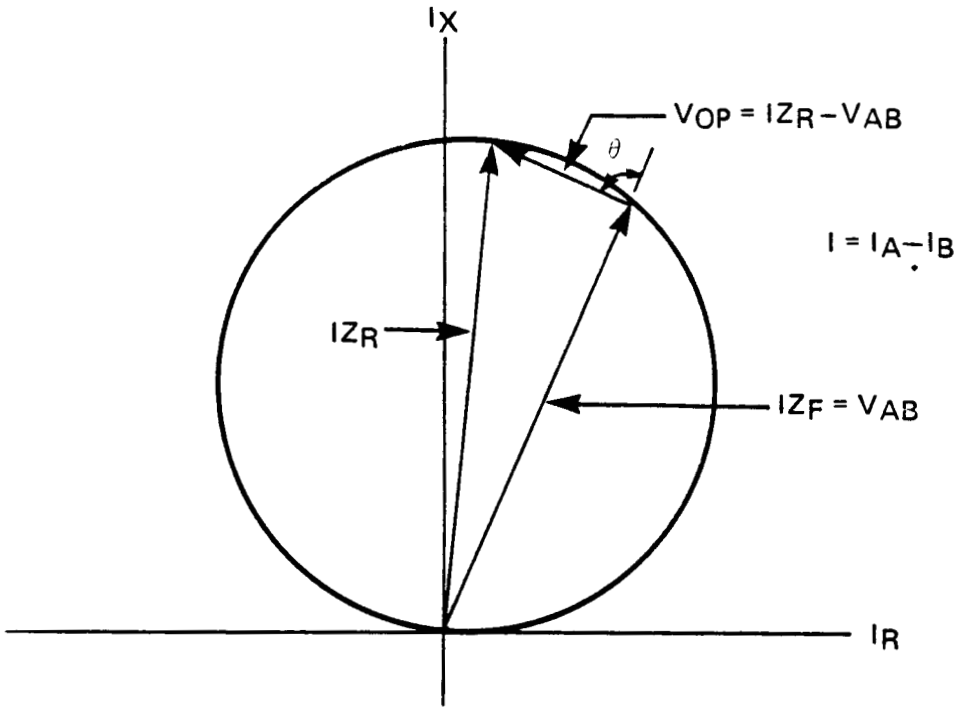


Fig. 3 Steady-State Mho Characteristic

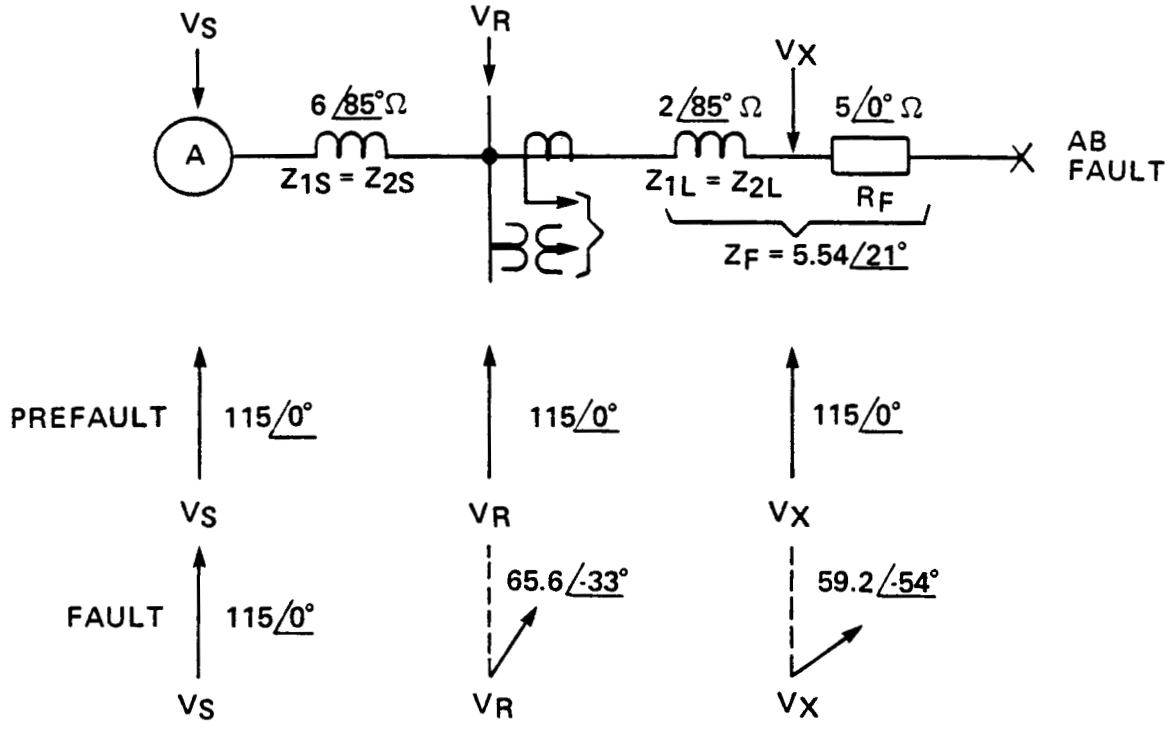


Fig. 4 System Arrangement, with Prefault and Fault Voltages. Secondary Impedance and Voltage Values Shown.

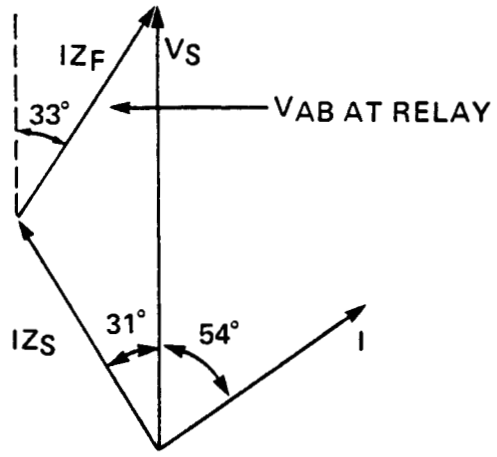


Fig. 5 Voltage Drops for System of Fig. 4

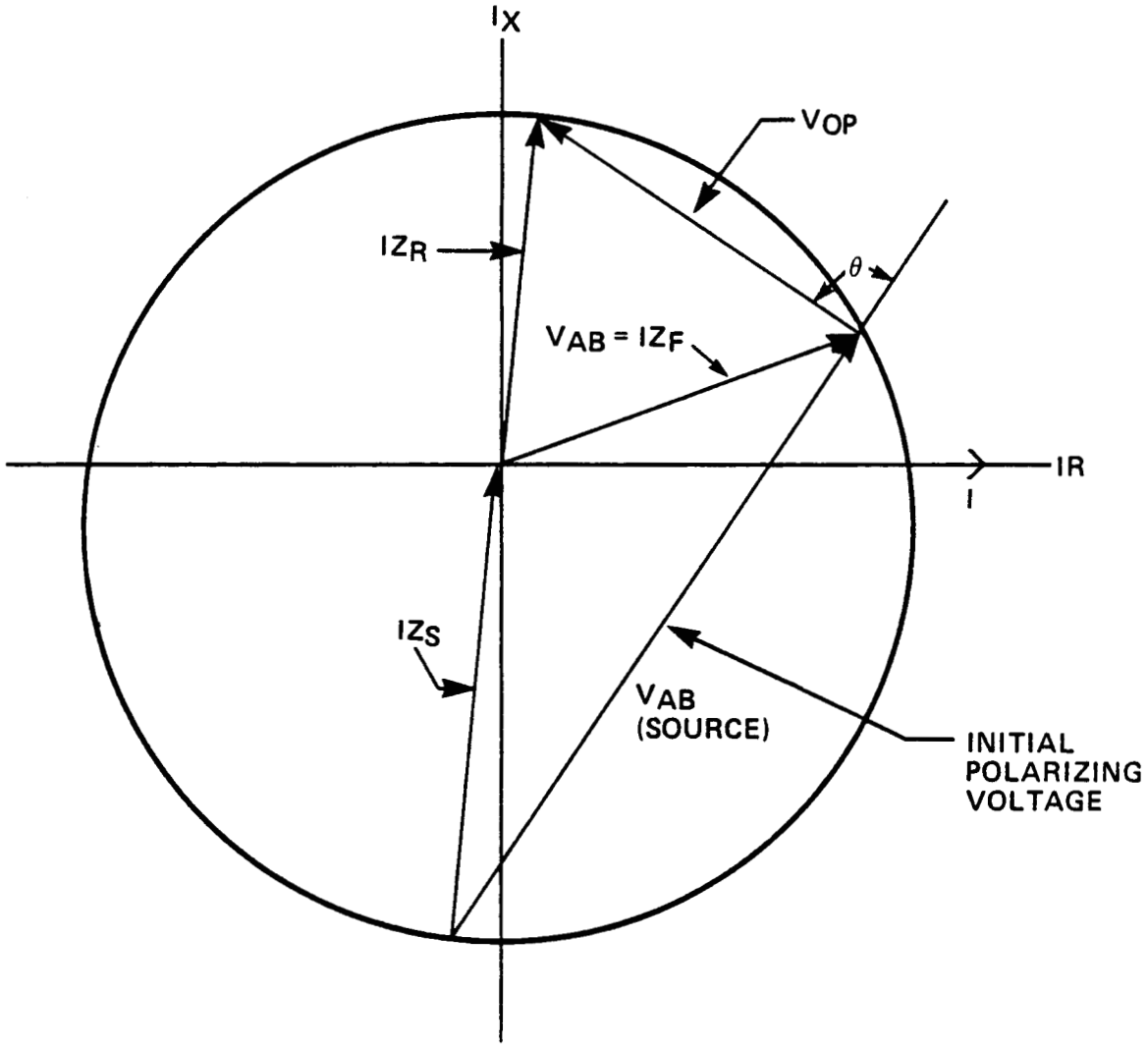


Fig. 6 Dynamic Mho Characteristic, Based on Conditions of Fig. 4

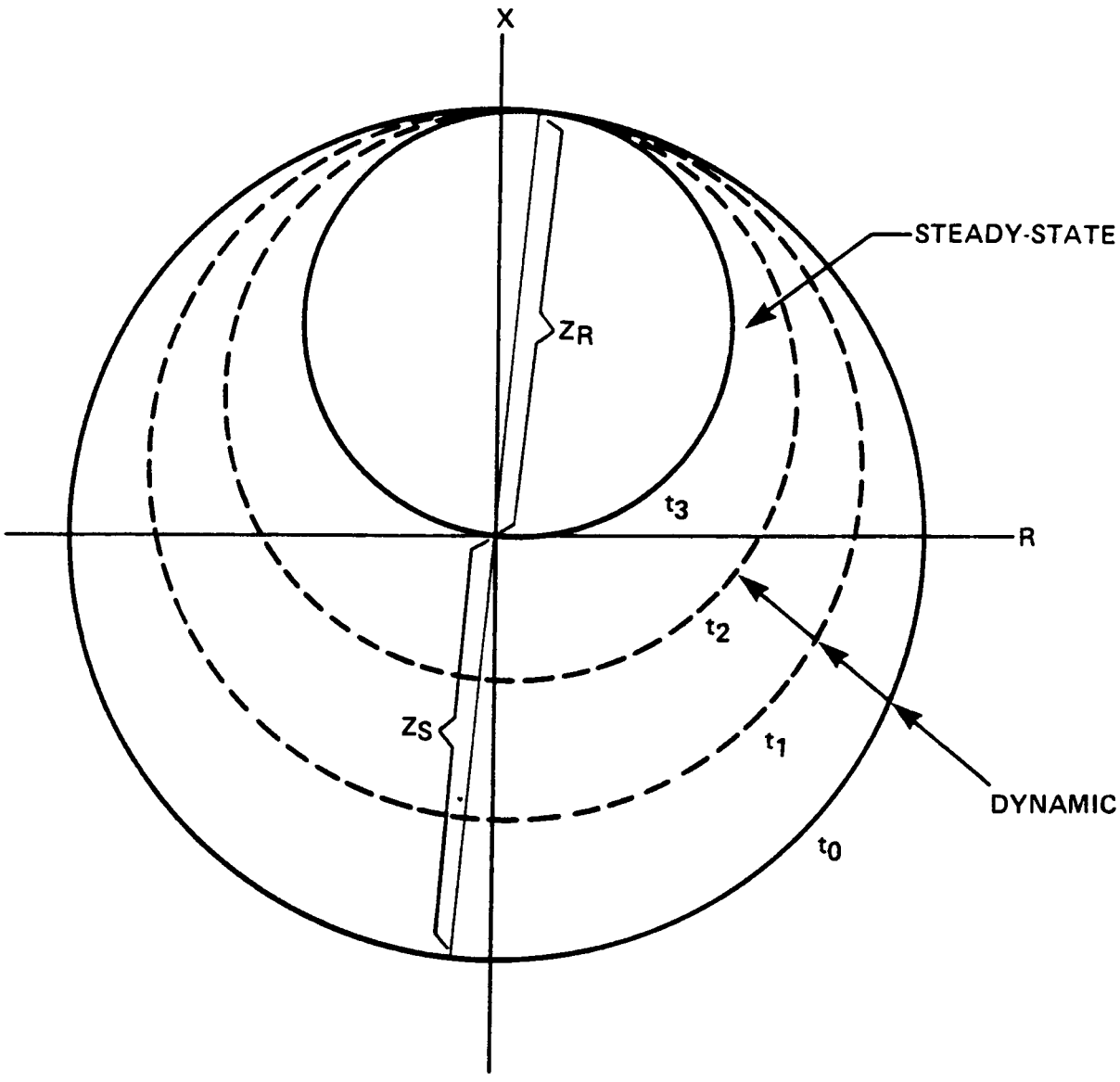


Fig. 7 Transition from Dynamic Characteristic to Steady-State Characteristic

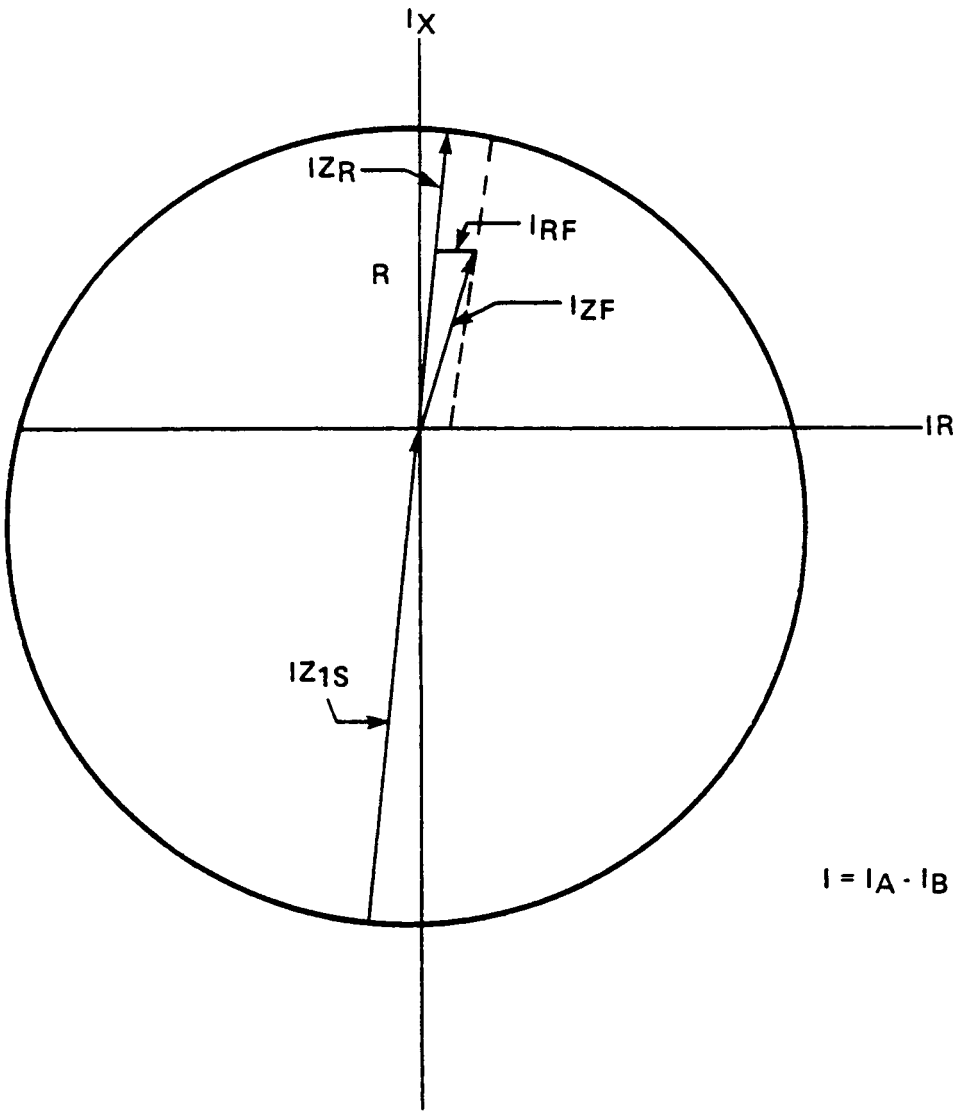


Fig. 8 Fault Resistance on Interphase Faults and Dynamic Characteristic

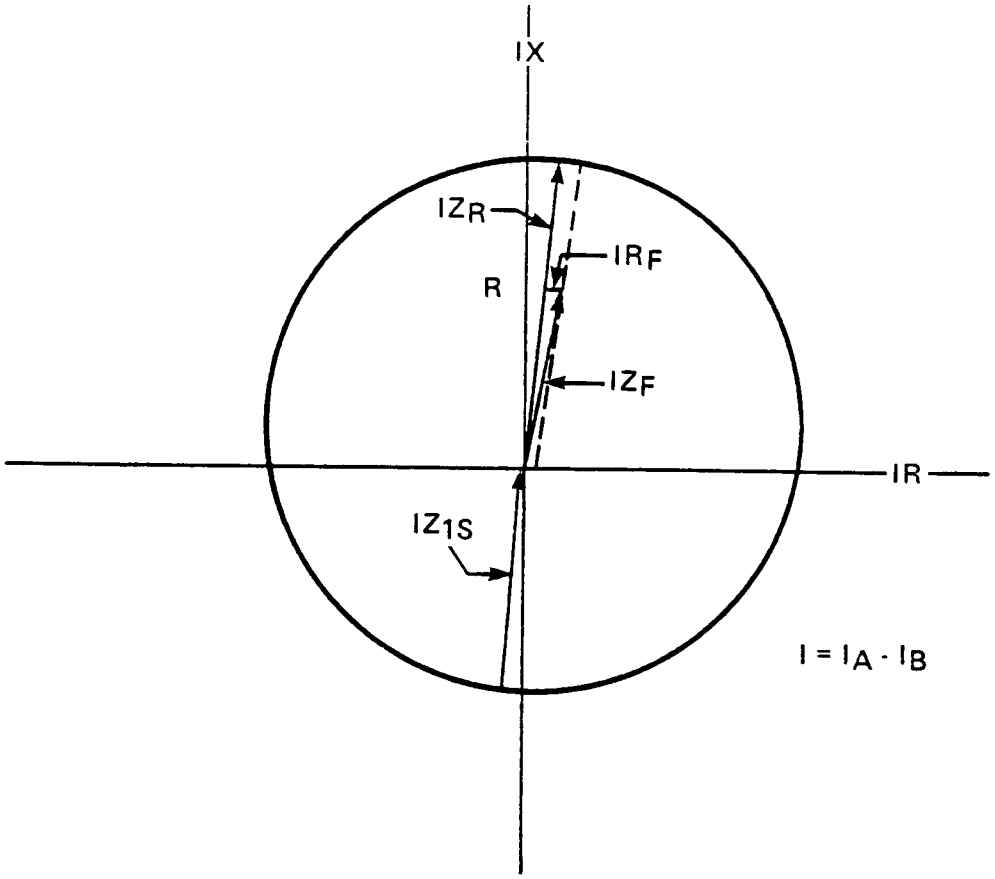


Fig. 9 Similar to Fig. 8 but with Smaller Source Impedance

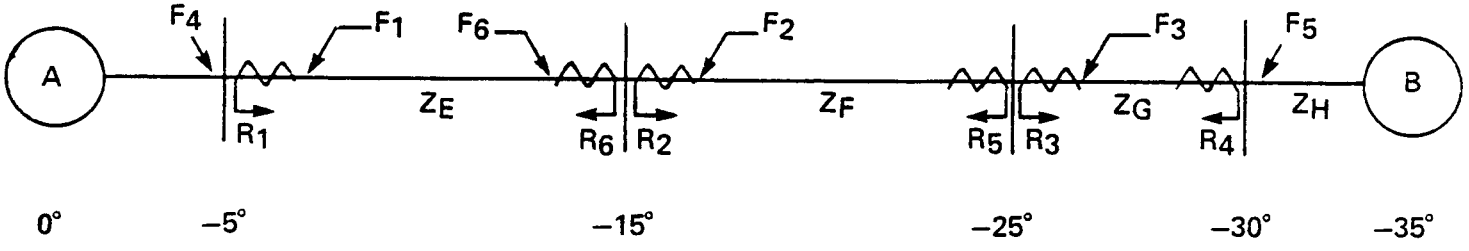


Fig. 10 Simple Two Machine System

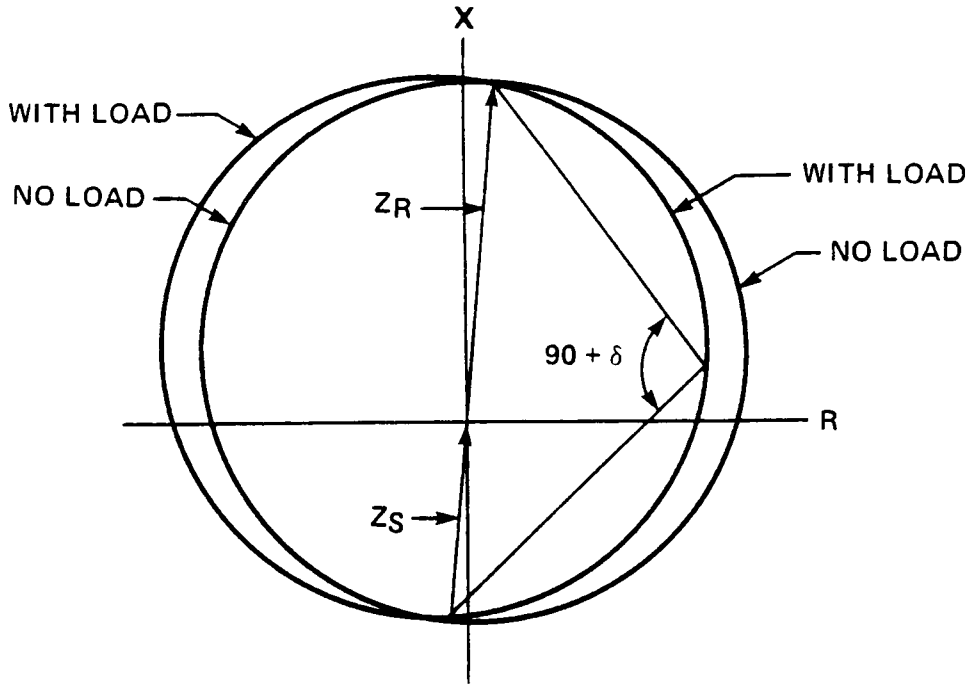


Fig. 11 Dynamic Characteristic With and Without Load

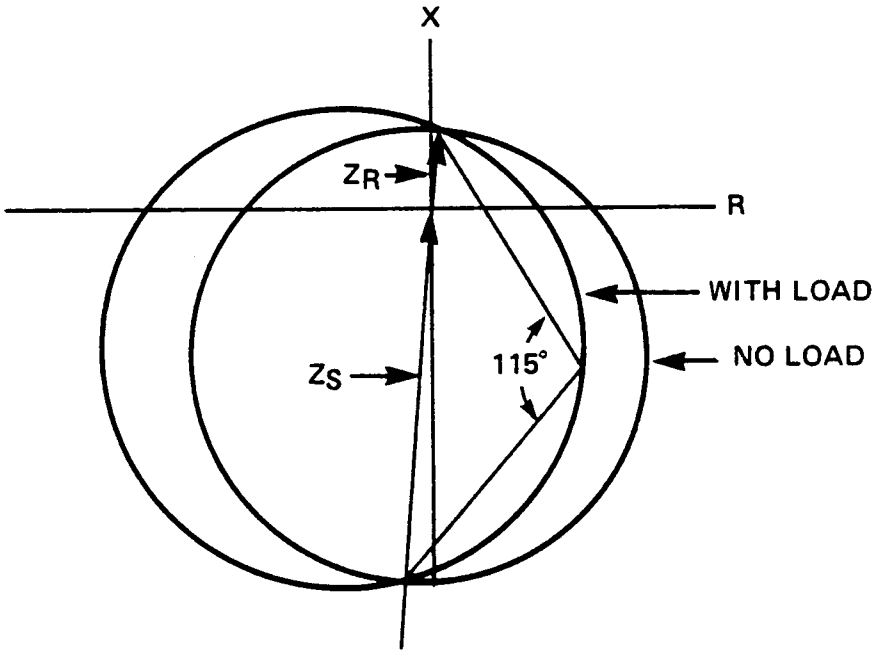


Fig. 12 Dynamic Characteristic for R3 Relay in Fig. 10, With and Without Load

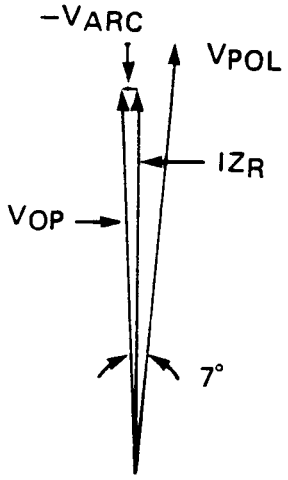


Fig. 13(a) Input Signals for R1 Relay, F1 Fault

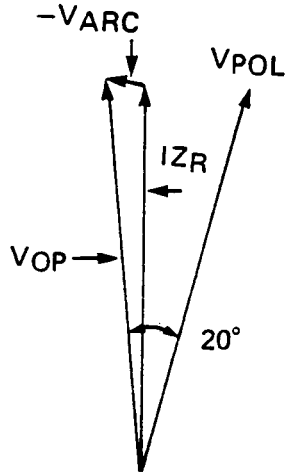


Fig. 13(b) Input Signals for R2 Relay, F2 Fault

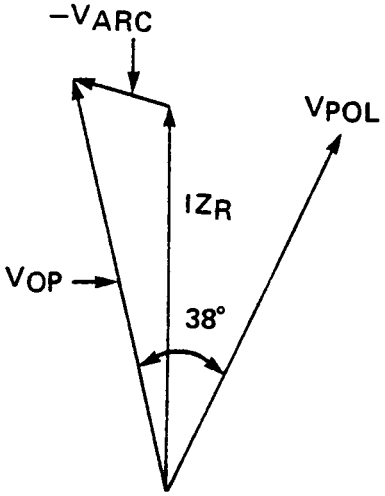


Fig. 13(c) Input Signals for R3 Relay, F3 Fault

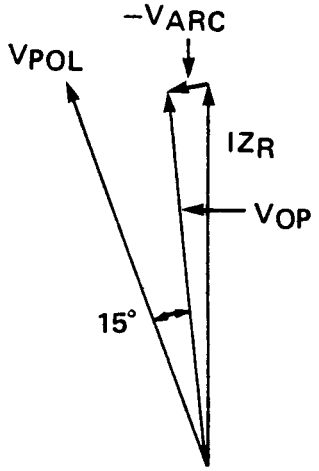


Fig. 13(d) Input Signals for R6 Relay, F6 Fault

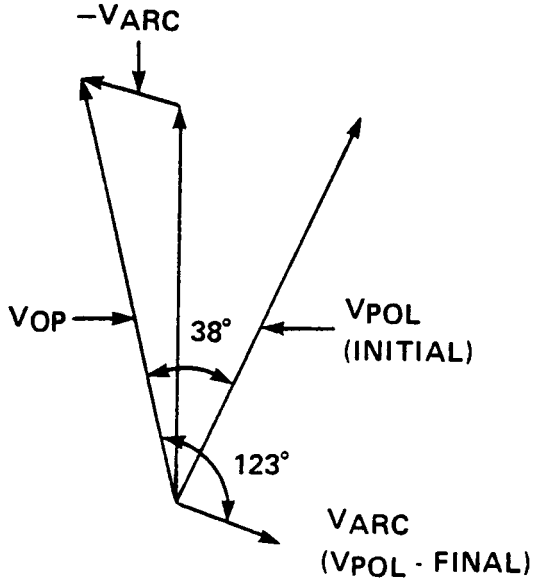


Fig. 14 Steady-State Angle Between V_{OP} and V_{ARC} for R3 Relay, F3 Fault, With Load Flow as in Fig. 10

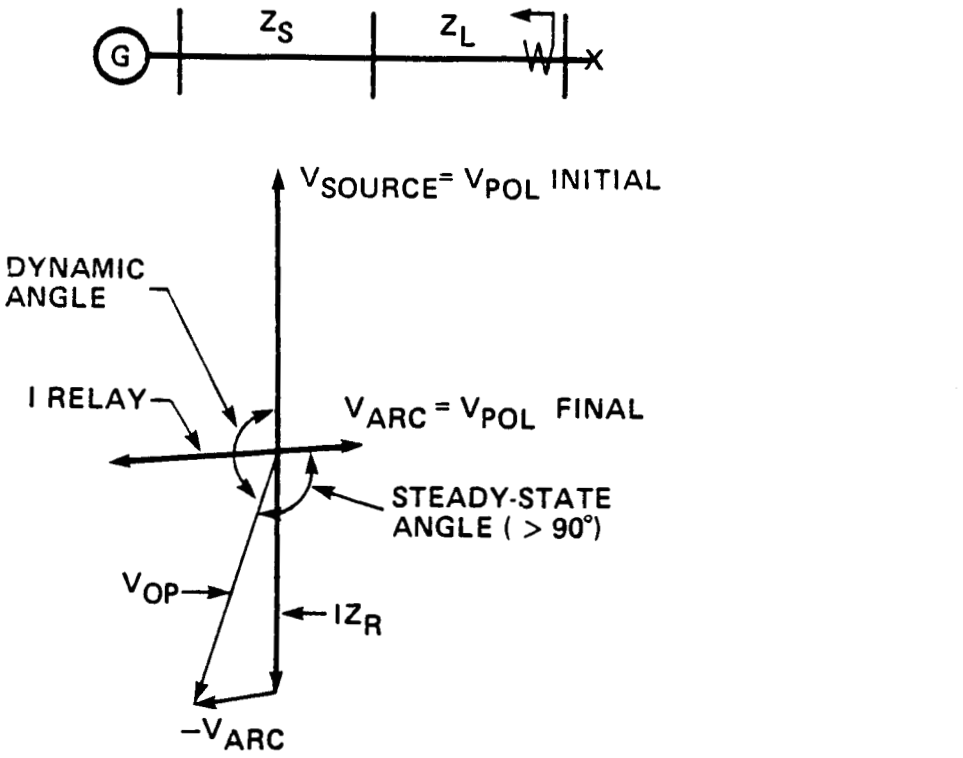


Fig. 15 Polarizing and Operating Phasors for Reverse Direction Fault, Radial Feed

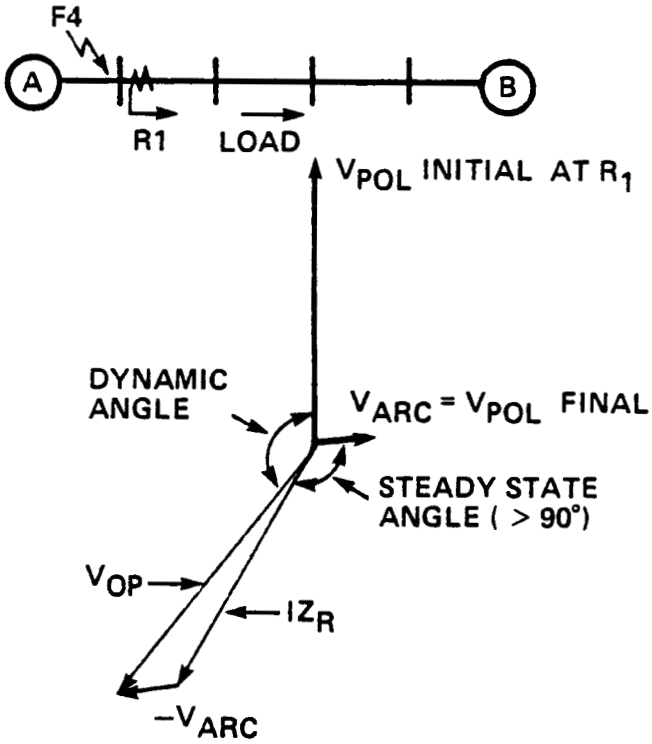


Fig. 16 Phasors for R1 Relay and F4 Fault, Load Flow in Tripping Direction

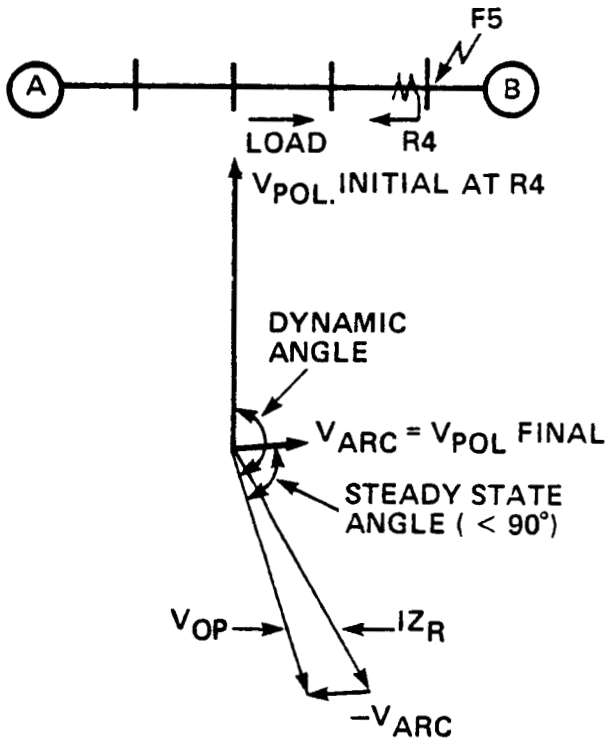


Fig. 17 Phasors for R4 Relay and F5 Fault, Load Flow in Non-Tripping Direction

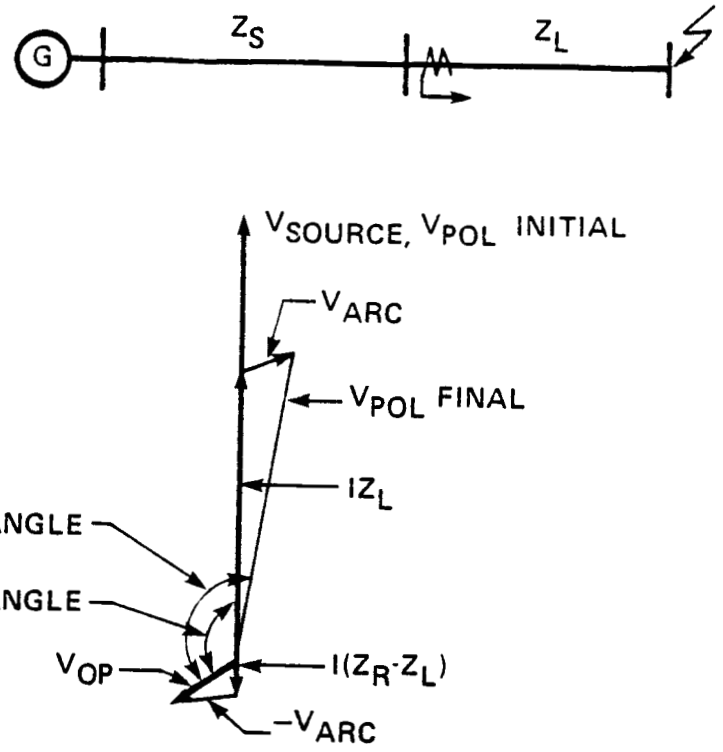
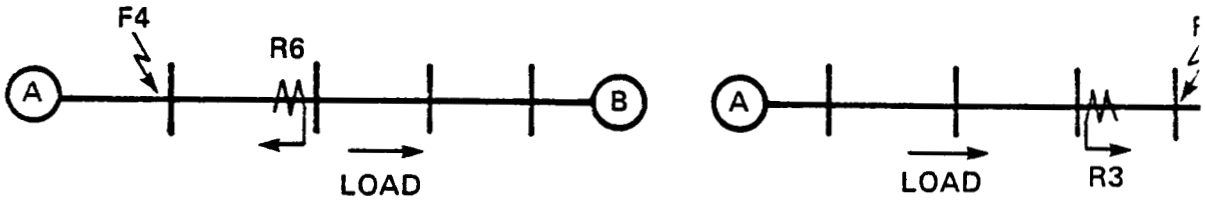


Fig. 18 Polarizing and Operating Phasors for First Zone Relay Set at 90% Z_L, for Fault at the End of the Line, No Load



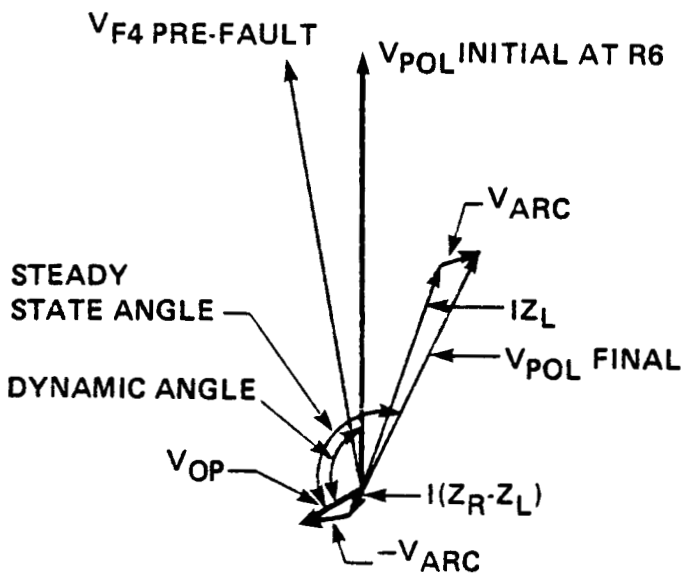


Fig. 19 Phasors for R6 Relay Zone 1 Setting, for Fault at F4

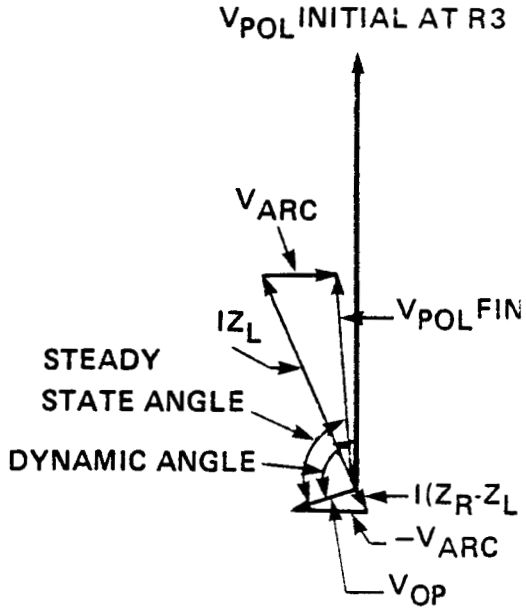


Fig. 20 Phasors for R3 Relay Zone 1 Setting, for Fault at F5